IN THE SPECIFICATION

Please replace paragraph **[0002]** with the following amended paragraph:

Figure 1a shows a memory core 101a. Typically, a memory core 101a is constructed with Dynamic Random Access Memory (DRAM) or Static Random Access Memory (SRAM) cells that store binary information (i.e., a "1" or "0"). For RAM cells, binary information is written to the cells via the Data_In input 102 and Information is read from the cells via the Data_Out output 104.

A1

Please replace paragraph **[0003]** with the following amended paragraph:

Other forms of cells that may be used to construct memory core 101a include Content Addressable Memory (CAM) cells and Read Only Memory (ROM) cells. CAM cells are designed to look for a "match" between stored information and offered information. As such, offered information is presented at the Data_In input 102 and the address location of matching data is presented at the Data_Out output 104. ROM cells are typically programmable. As such, the information to be programmed is entered at the Data_In input 102 and read from the Data_Out output 104.

A2

Please replace paragraph **[0004]** with the following amended paragraph:

Regardless of the type of memory cell used to construct memory core 101a, both the Data_In input 102 and the Data_Out output 104 typically take the form of a bus that holds a plurality of bits. As such, multiple cells may be simultaneously written to or read from. The address bus 103 is used to identify the particular group of cells that are simultaneously written to or read from. A read enable (RE) 190 is

A3

a3 active during a memory read and a write enable (WE) 191 is active during a memory write.

Please replace paragraph **[0022]** with the following amended paragraph:

That is, the memory unit 250a behaves according to the operation of the memory core 201a. Note the presence of multiplexers 207a,b and multiplexer ~~214a~~ respectively coupled to the memory core data input 202, the memory core address input 203 and the memory core data output 204. During normal operational mode, the Test_Enable (TE) is inactive which configures: 1) multiplexer 207a to select the Data_In input 205 (which may be referred to as a system data input); and 2) multiplexer 207b to select the address input 206 (which may be referred to as a system address input).

a4

Please replace paragraph **[0032]** with the following amended paragraph:

During a preload write stage the test data and address offered by the test controller 209a<u>b</u> are latched by registers within each interface 258, 260. That is, the test data is latched by registers 244, 245 and 246 within the Data_In interface 258 and the address is latched by analogous registers within the address interface 260. During a preload read stage, the appropriate address is latched into the same analogous registers within the address interface 260.

a5

Please replace paragraph **[0033]** with the following amended paragraph:

During a second stage, which is either a write operation or a read operation: 1) (for a write operation) the write enable inputs are activated by the test controller 209b for those ports that are to be written to (e.g., WE_A 290 for port A, WE_B 291 for port B, and WE_C 292 for port C) and data is written into the port from either the register or the test controller 209b (depending on the value of the Shadow_Sel signal for each activated port); 2) (for a read operation) data is read from the multi-port memory core 201b from those ports whose read enable lines are activated by the test controller 209b.

Please replace paragraph **[0034]** with the following amended paragraph:

For either read or write operations the appropriate address for the operation, depending upon the value of the Shadow_Sel signal for the enabled port, is released from a register within the address interface 260 or is sent from the test controller 209b. The Shadow Sel signals (e.g., ShadowA_Sel 274 for port A, ShadowB_Sel 275 for port B, ShadowC_Sel 276 for port C), multiplexers 295, 296, 297 and registers 244, 245, 246 allow test data directed to a particular "target port" to be directed to a port other than the target port in the following write operation.

Please replace paragraph **[0035]** with the following amended paragraph:

A target port corresponds to the port being written into by the test controller directly on a given write operation. For example, if port C is the target port for a particular write operation, the ShadowC_Sel 276 signal is positioned to force

multiplexer 297 to select the Test Data_In 210b from the test controller 209b (rather than register ~~297~~246). As such, the data on the Test Data_In 210b line is written into port C.

Please replace paragraph **[0044]** with the following amended paragraph:

The data field 303 provides data to be written into the memory core in those port(s) and/or byte(s) specified by a WRITE command. The data field 303 also provides data that was read from the memory from those port(s) and/or bytes(s) specified by a READ command. Note, therefore, that the command format 300 of Figure 3 may also correspond to an output presented at the Test_Out output 213 of the controller 209b. That is, for READ commands, the controller presents information (e.g., in the form of command format 300 of Figure 3) as part of the actions performed in response to the test command. The command field 301 may be used to specify that the appended information corresponds to controller output data.

Please replace paragraph **[0050]** with the following amended paragraph:

Furthermore, those "remainder" ports that are not pointed to by the PORTID (e.g., ports A and B if the PORTID points to port C as the target port) may be simultaneously written to with the contents of their respective registers (e.g., register ~~245~~ 244 for port A and register ~~246~~ 245 for port B). Whether or not a remainder port is to be written to is specified, in an embodiment, by a fifth partition of the location field 302. That is, the location field 302 may be further partitioned into a fifth

reserved section (referred to as the SMASK) that specifies which remainder ports are written to be with register contents and which remainder ports are not to be written to at all during this write cycle operation.

A10

Please replace paragraph **[0055]** with the following amended paragraph:

Regardless of the type of the core employed, the data received from the memory core is presented at the controller output (e.g., at the Test_Out output 213 seen in Figure 2b). In an embodiment, the data is presented at the controller output in a format similar to the command format seen in Figure 3. The command field 301 specifies the data located in the data field 303 is an output of the controller that has resulted from a memory core read.

A11

Please replace paragraph **[0059]** with the following amended paragraph:

The testing versatility of each memory core (as offered by each memory unit 450a, 450b through 450N) allows for robust system level testing. That is, for example, "debug" testing during product development or "functional quality and assurance" testing during product manufacturing may take advantage of the ability to write various combinations of data patterns in order to effectively "jump start" the system to a particular state (e.g., a particular location of a particular software program).

A12